R15

Code No: 124DT

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year II Semester Examinations, February - 2024
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART - A

(25 Marks)

1.a)	What is Gray code? List out limitations of it.	[2]
b)	How do you obtain dual of an expression? Give suitable example.	[3]
c)	What are merits of K-map method?	[2]
d)	Design a full adder using two half address.	[3]
e)	Compare latch and flip flop.	[2]
f)	Explain the timing considerations of sequential circuits.	[3]
g)	What are the basic types of shift registers?	[2]
h)	Compare asynchronous and synchronous counters.	[3]
i)	Define finite state machine.	[2]
j)	What is an ASM chart? Explain.	[3]

PART - B

(50 Marks)

2.a) Convert the given Gray code number to equivalent binary 001001011110010.
b) Convert $(A0F9.0EBA)_{16}$ to decimal, binary, octal. [4+6]

OR

3.a) Obtain dual of the following Boolean expressions i) AB+A(B+C)+B′(B+D)
ii) A+B+A′B′C.
b) Obtain the compliment of the following Boolean expressions
i) A′B+A′BC′+A′BCD+A′BC′D′E
ii) ABEF+ABE′F′+A′B′EF. [5+5]

4.a) Define i) Prime implicants ii) Essential prime implicants.
b) Minimize the following expression using K-map and realize using NOR Gates.
$f = \pi M(0,4,6,7,8,12,13,14,15)$. [4+6]

OR

5.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
b) Realize the function $f(A,B,C,D)=\pi(1,4,6,10,14)+d(0,8,11,15)$ using: i) 16:1 MUX ii) 8:1 MUX. [4+6]

6.a) What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.

b) Explain the realization of SR flip-flop, JK flip-flop using D flip-flop. [5+5]

OR

7.a) Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.

b) Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits. [5+5]

8.a) Discuss about synchronous and ripple counters. Compare their merits and demerits.

b) What do you mean by universal shift register? Draw and explain its circuit diagram and operation. [5+5]

OR

9.a) What is a shift register? Explain about the following modes of operations in a four bit shift register (i) shift right (ii) shift left (iii) bidirectional.

b) Design and construct MOD-5 synchronous counter using JK flip flops. [6+4]

10.a) What are the capabilities and limitations of finite state machines? Discuss.

b) What are the Moore and Melay machines? Compare them. [5+5]

OR

11.a) Name the elements of an ASM chart and define each one of them.

b) Explain the control subsystem implementation of weighing machine. [5+5]

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